

# *PWWAA*

## *Marseille LC*

# L-A6841P REV 0.1 Schematic

Intel Penryn/ Cantiga/ ICH9M  
2010-07-22 Rev. 0.1

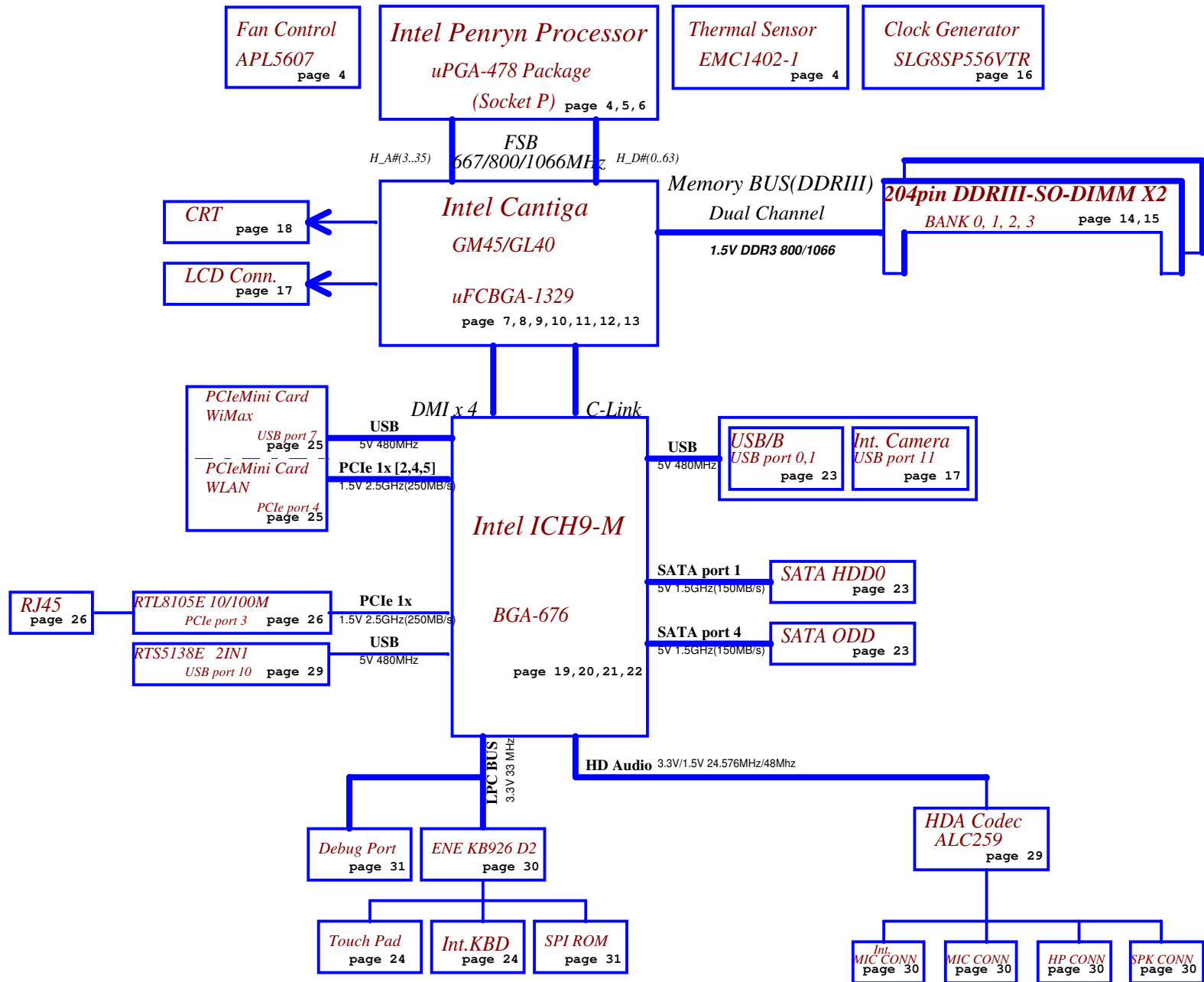
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# Compal Confidential

Model Name : PWWAA

File Name : LA-6841P



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RTC CKT.	page 20
DC/DC Interface CKT.	page 33
Power Circuit DC/DC	page 34, 35, 36, 37, 38, 39, 40

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## Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5 power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8V power rail	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for SB	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

## BTO Option Table

Function	Card Reader	Camera	WLAN	Energy Star
description		(X)	Always	Always
explain		Camera	WLAN	Energy Star
BTO		CAM@	WLAN@	

## External PCI Devices

DEVICE	PCI DEVICE ID	IDSEL#	REQ/GNT#	PIRQ
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## EC SM Bus1 address

## EC SM Bus2 address

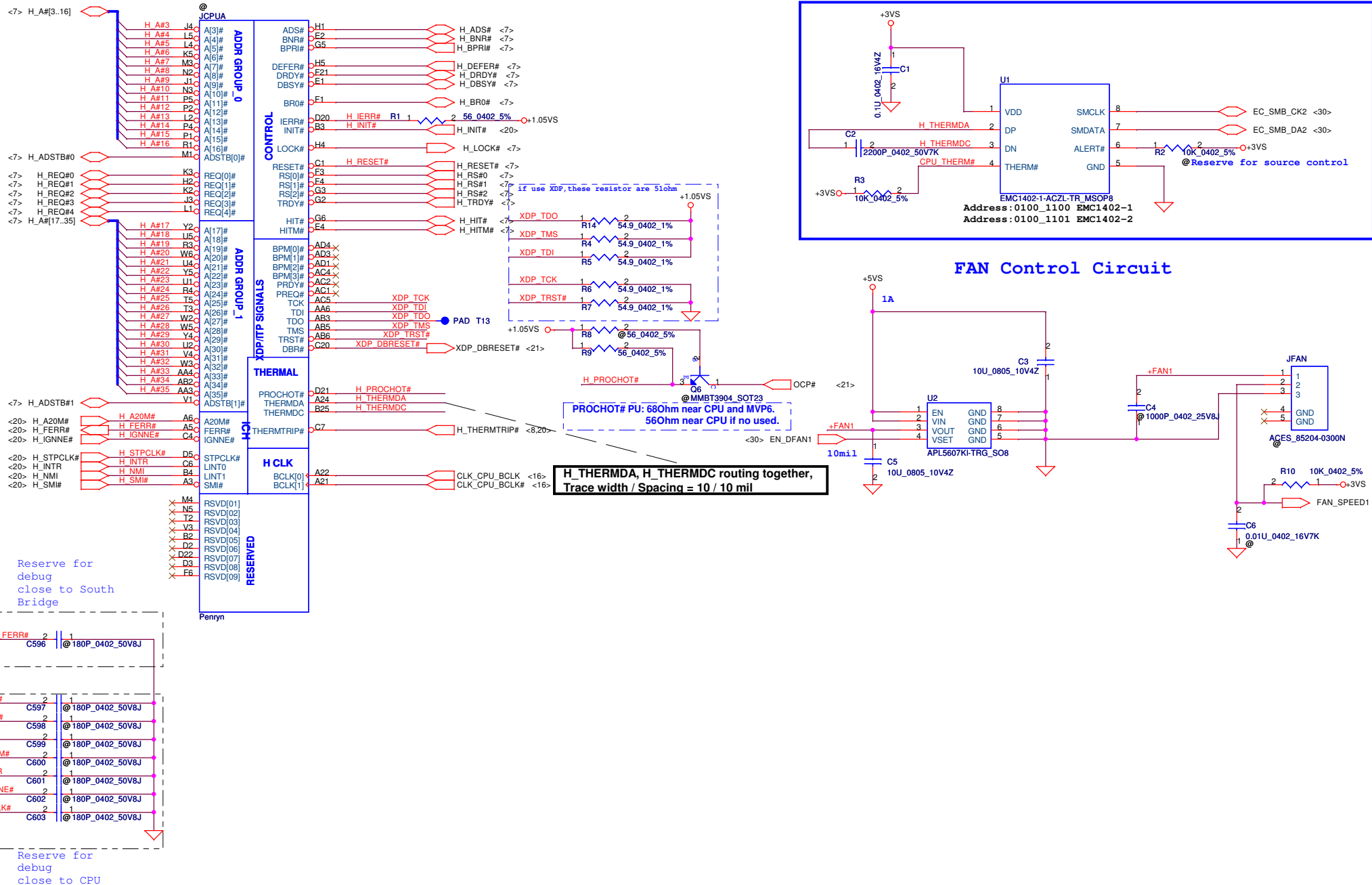
Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D2		+3VS	EC KB926 D2	
+3VL	Smart Battery	0001 011X b	+3VS	CPU THM Sen SMSC SMC1402	1001 101Xb

## ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb

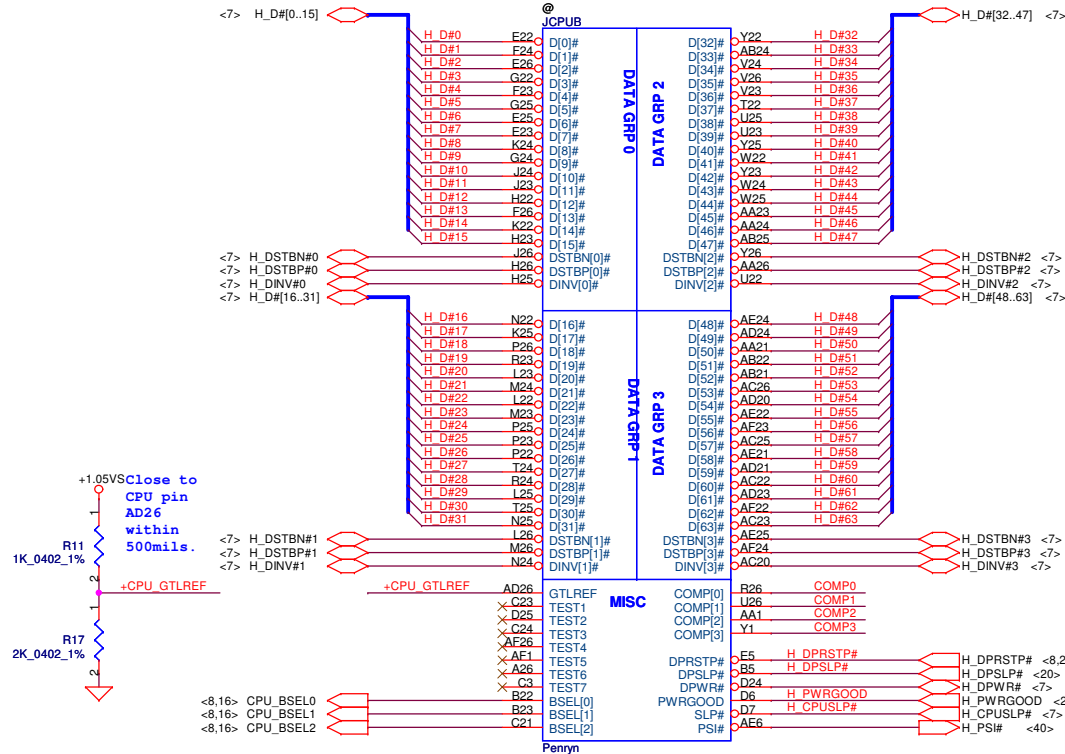
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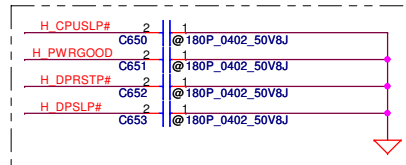
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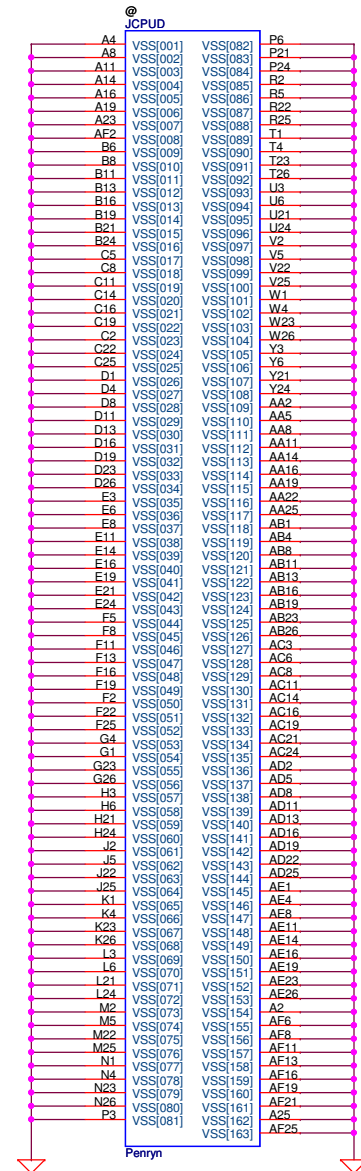


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



Reserve for debug close to CPU

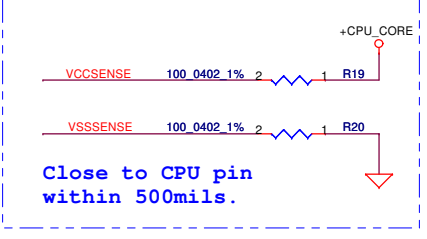
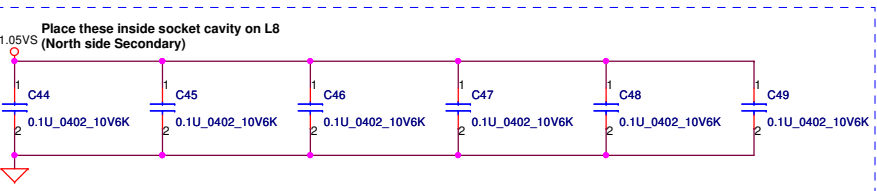
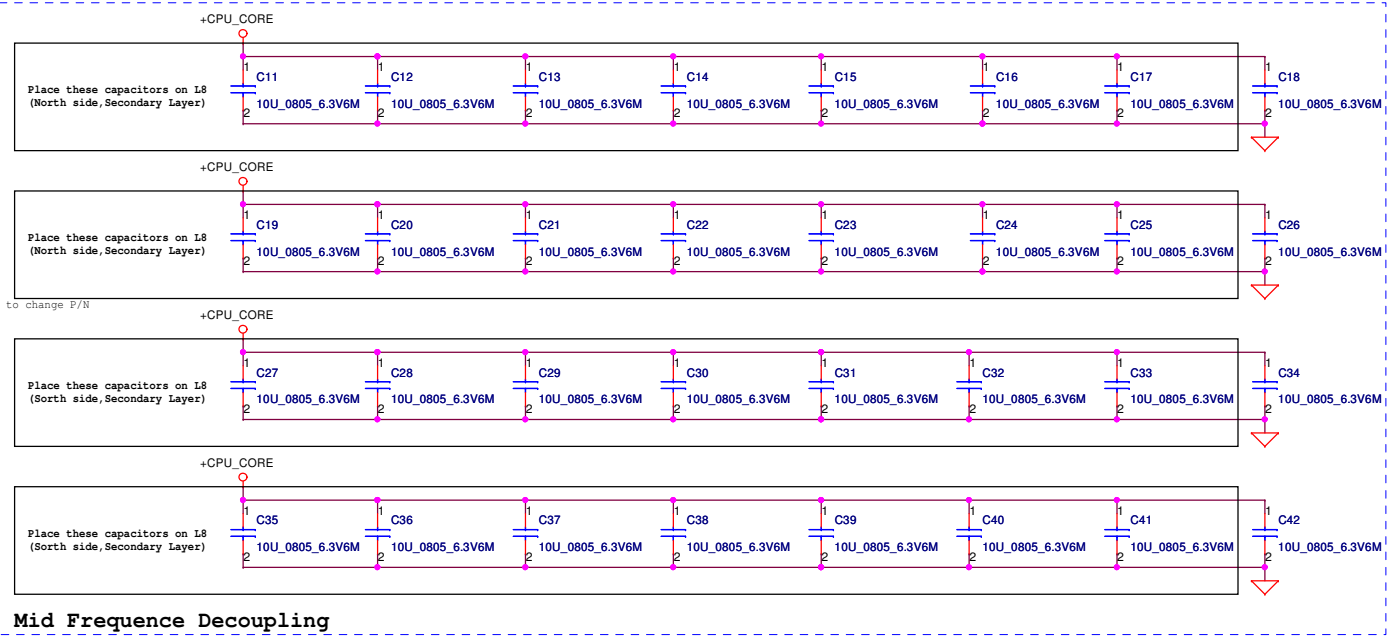
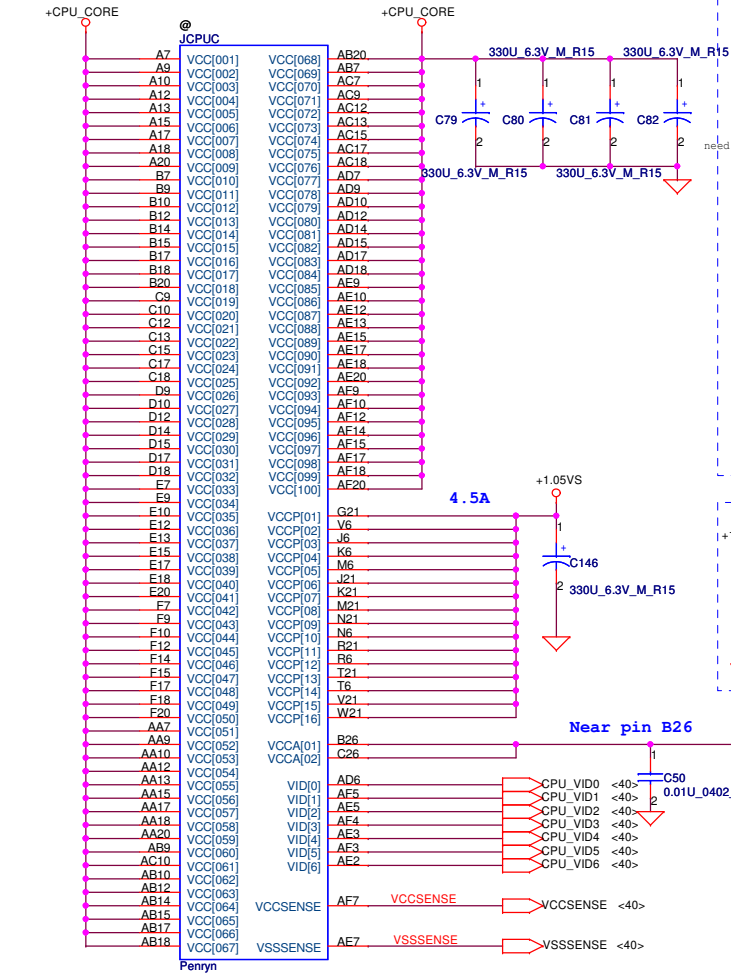


layout note: Please use "Daisy Chain" to layout and the signal (H\_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU



Near CPU CORE regulator

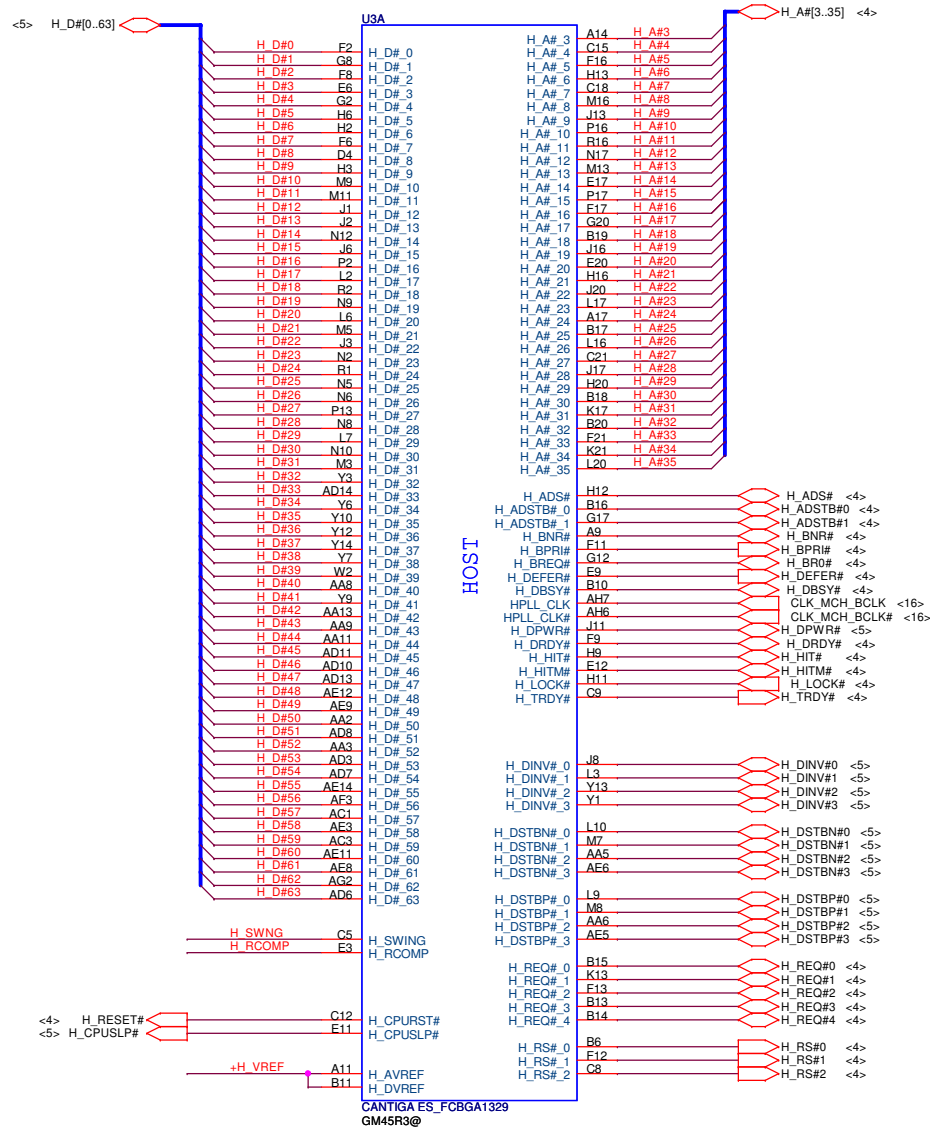
ESR <= 1.5m ohm  
Capacitor > 1980uF



Length match within 25 mils.  
The trace width/space/other is 14/7/25.

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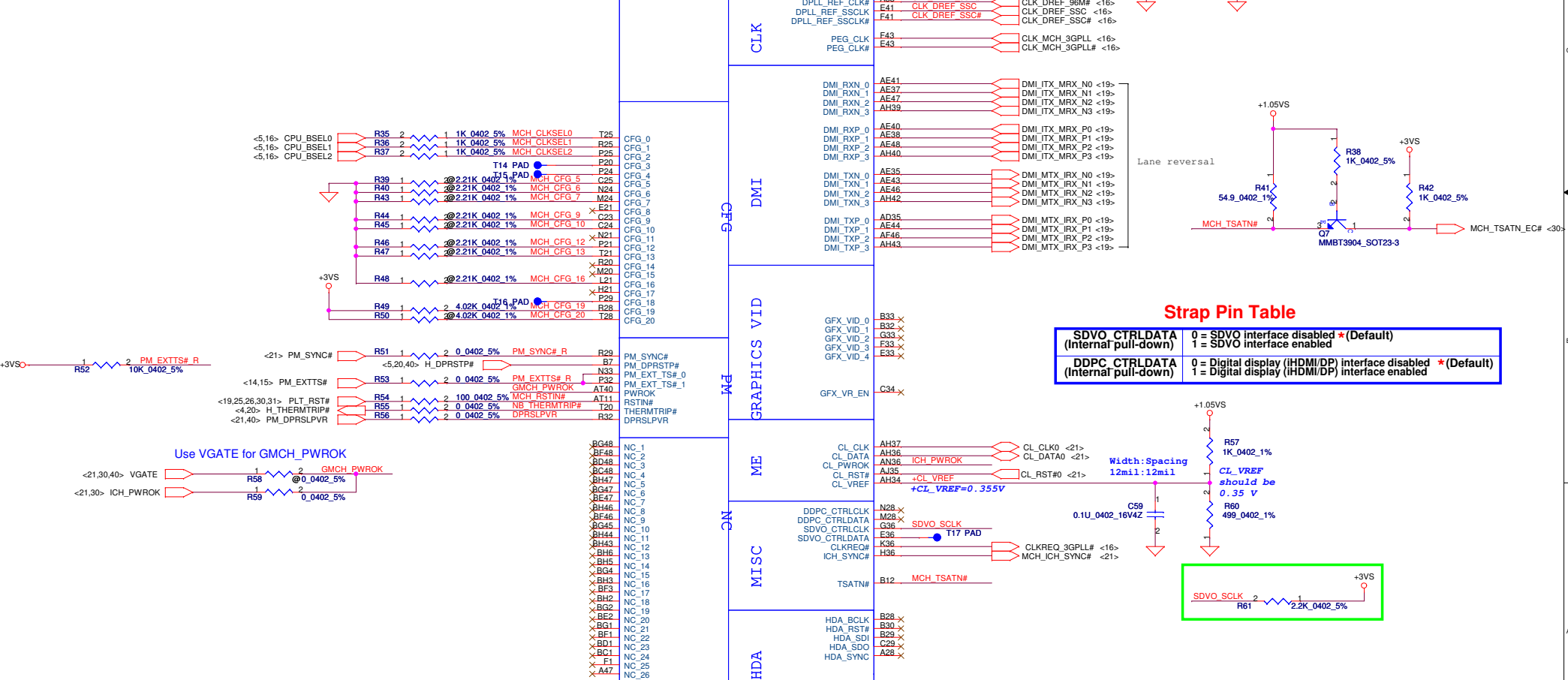


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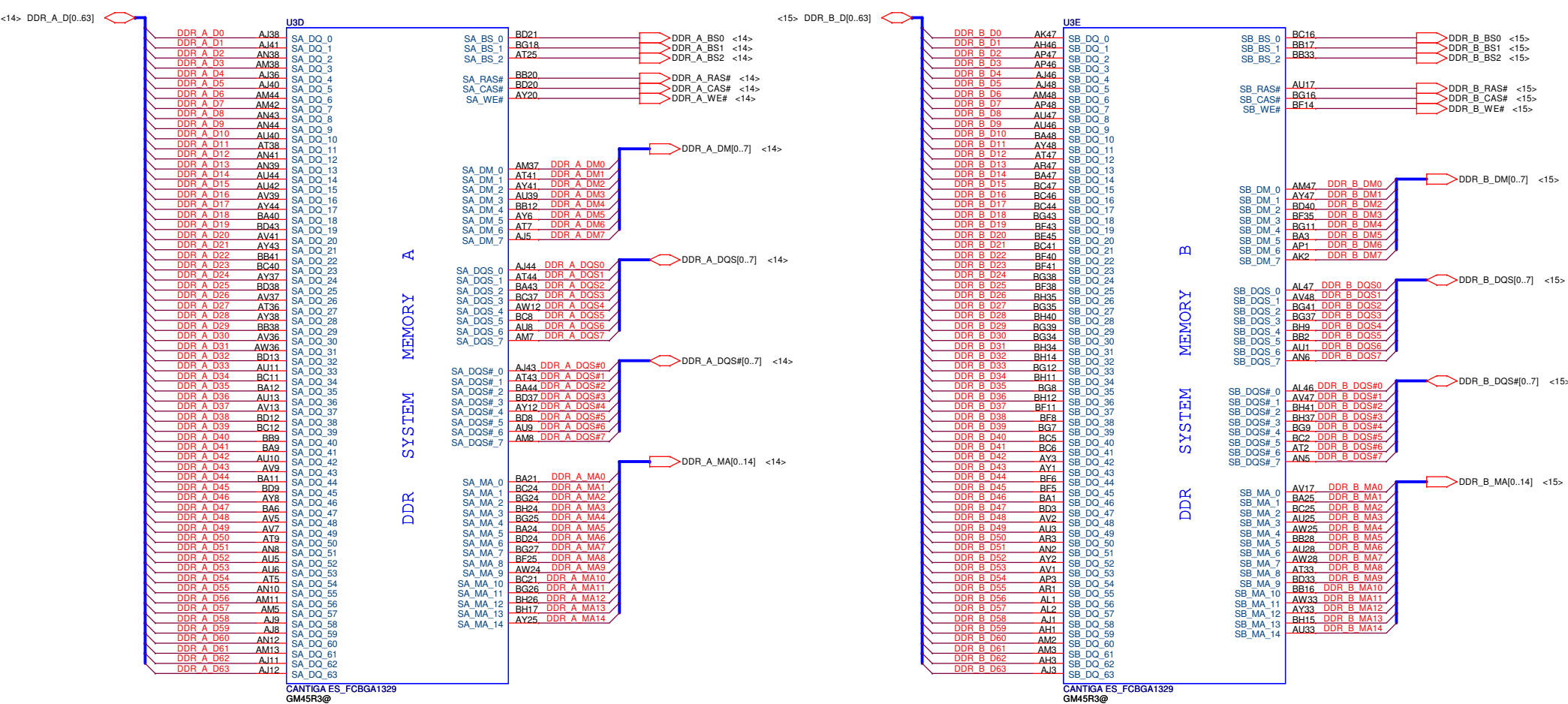


Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5 Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6 Internal pull-up	0 = ITPM Host Interface is enabled can support disble by SW. 1 = ITPM Host Interface is Disabled *(Default)
CFG7 Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9 Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10 Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12] Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16 Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19 Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 Internal pull-down (PCIe/SDVO select)	0 = Only PCIe or [SDVO/DP/HDMI] is operational. *(Default) 1 = PCIe/[SDVO/DP/HDMI] are operating simu.



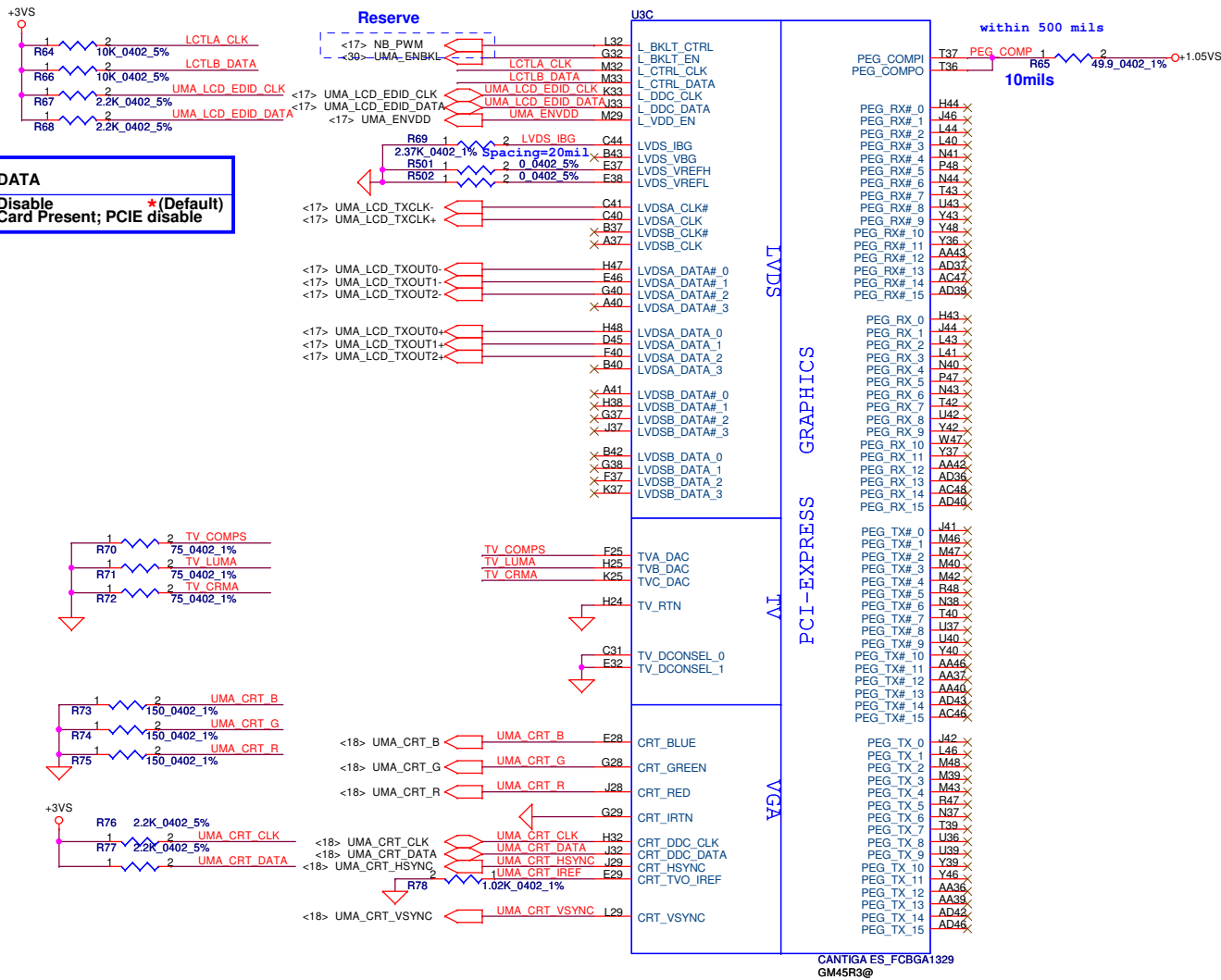




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**L\_DDC\_DATA**  
0 = LFP Disable  
1 = LFP Card Present; PCIE disable



CANTIGA ES\_FCBGA1329  
GM45R3@

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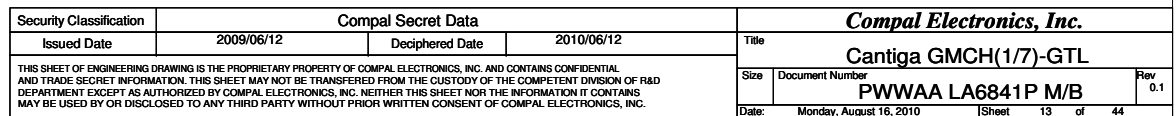








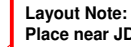




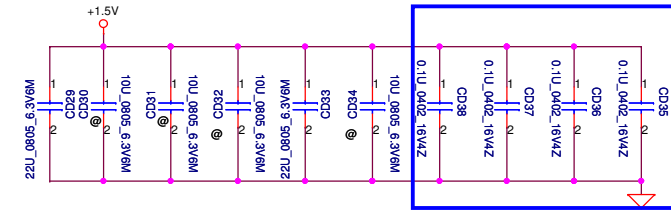




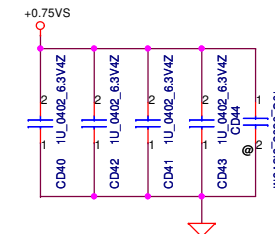




**Layout Note: Place these 4 Caps near Command and Control signals of DIMMB**



**Layout Note:**  
Place near JDDRL.203 & JDDRL.204

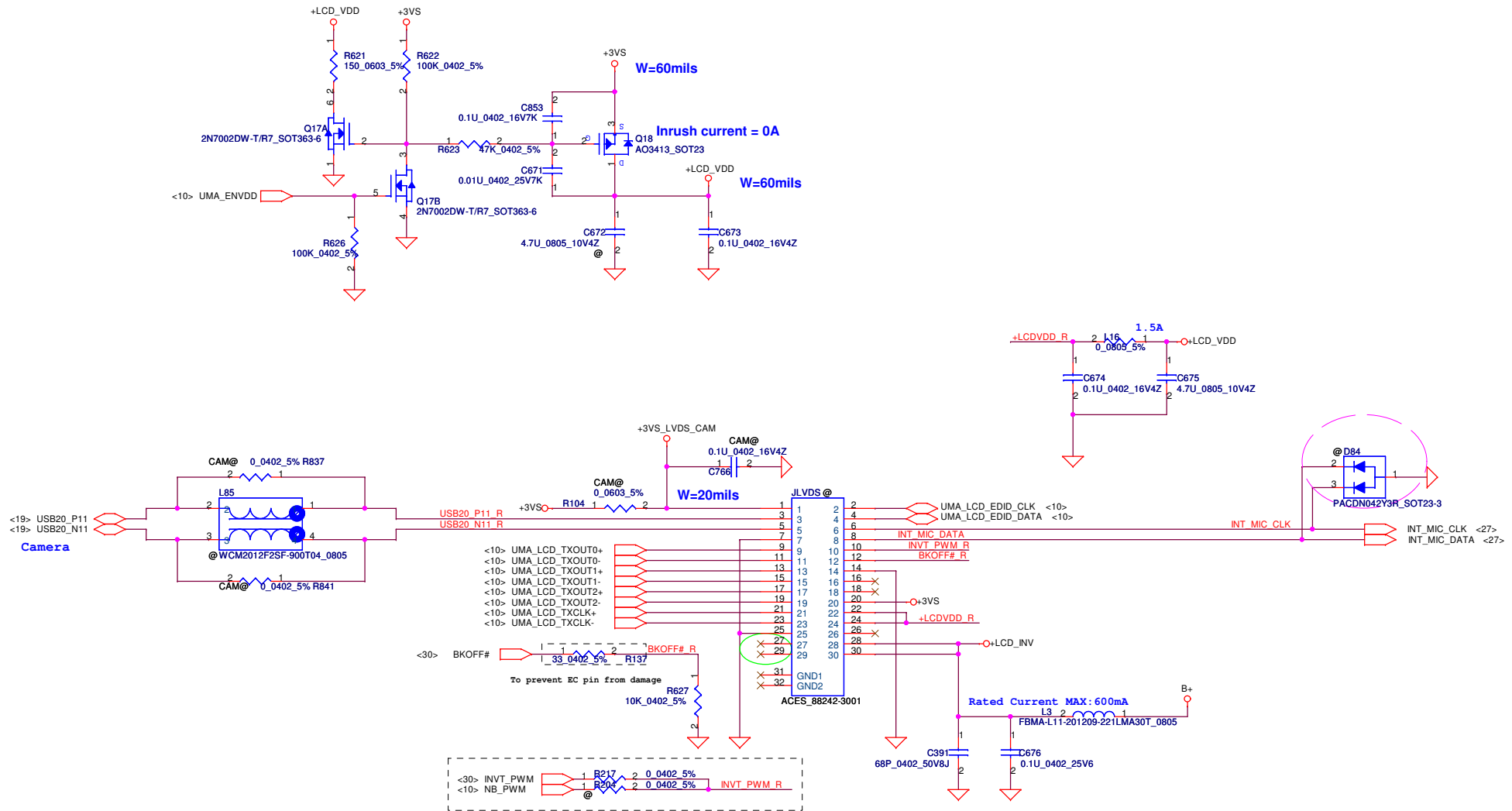








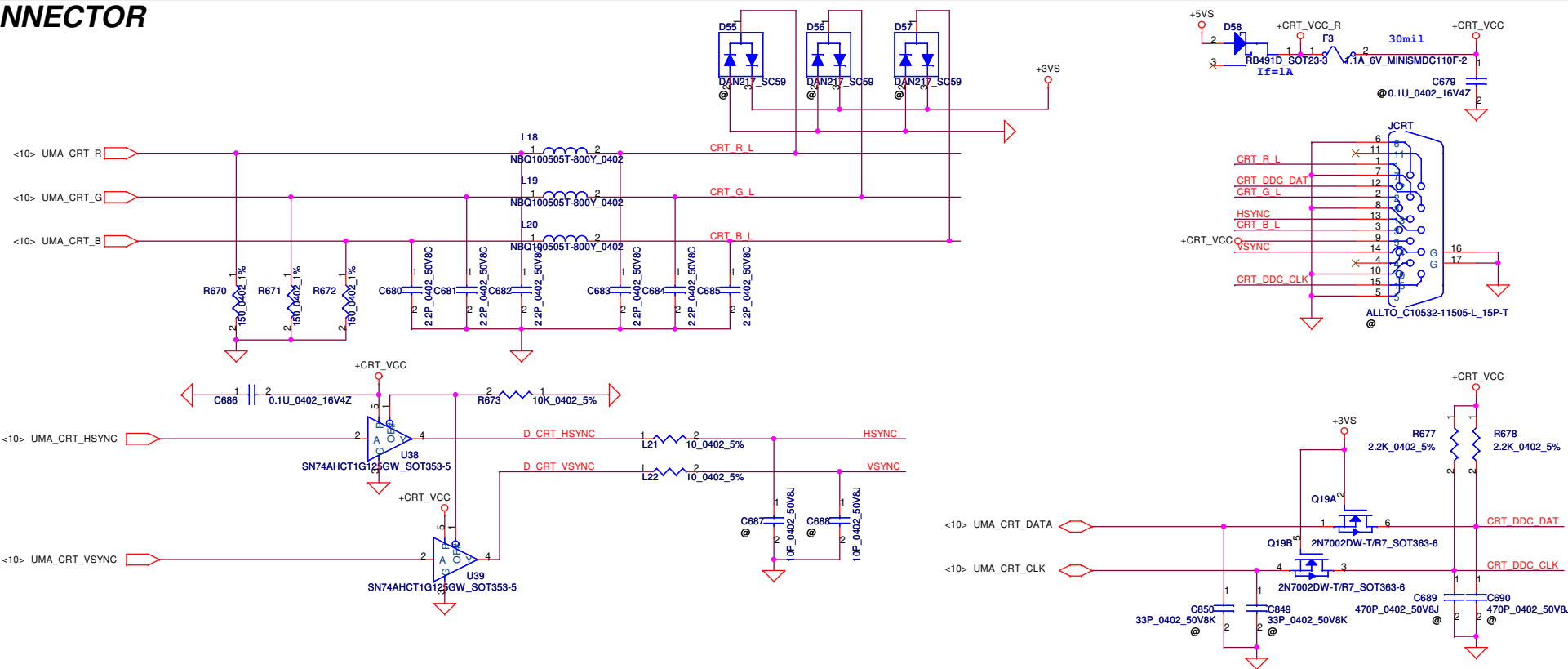
# LCD/PANEL BD. Conn.



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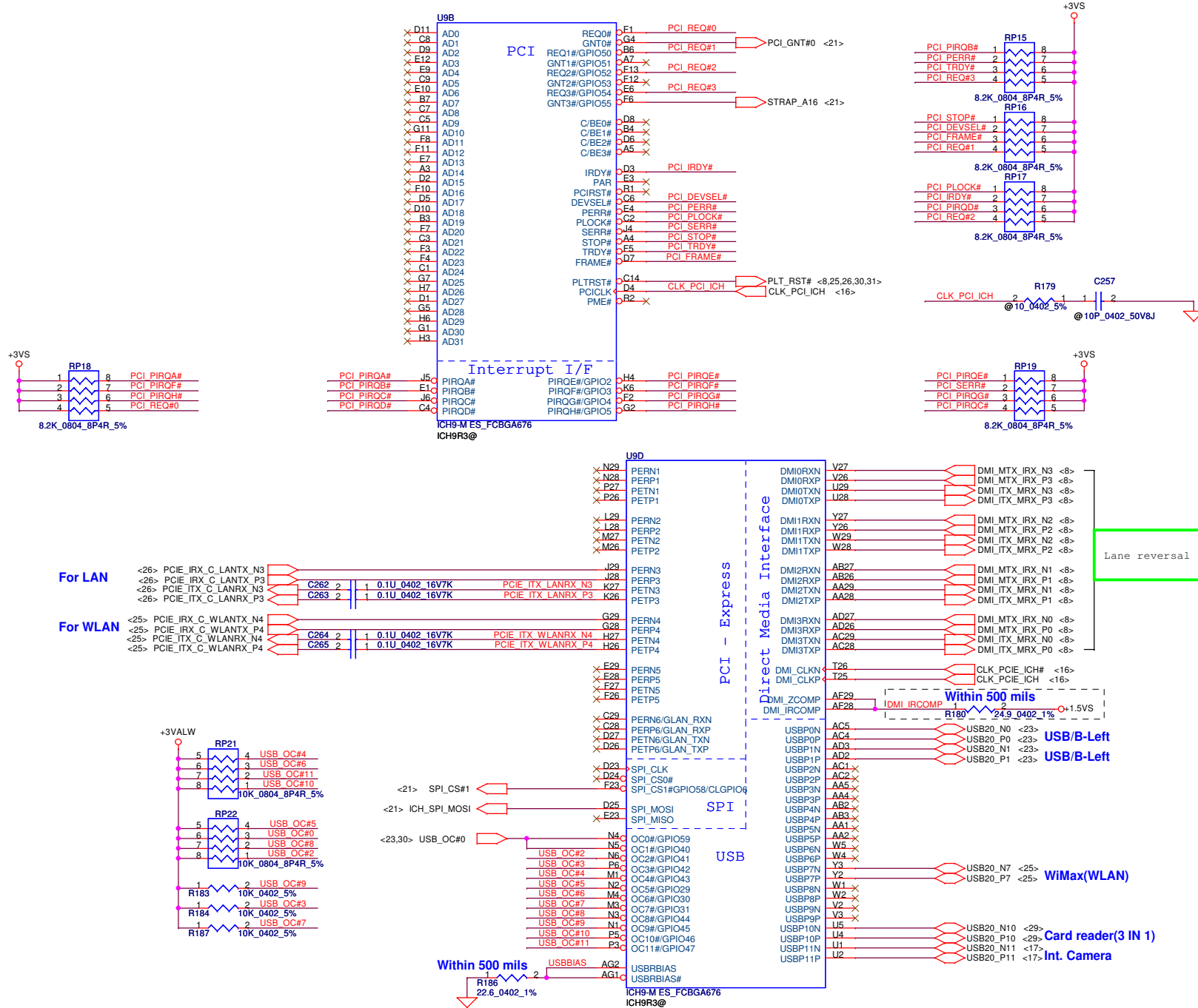
CRT CONNECTOR



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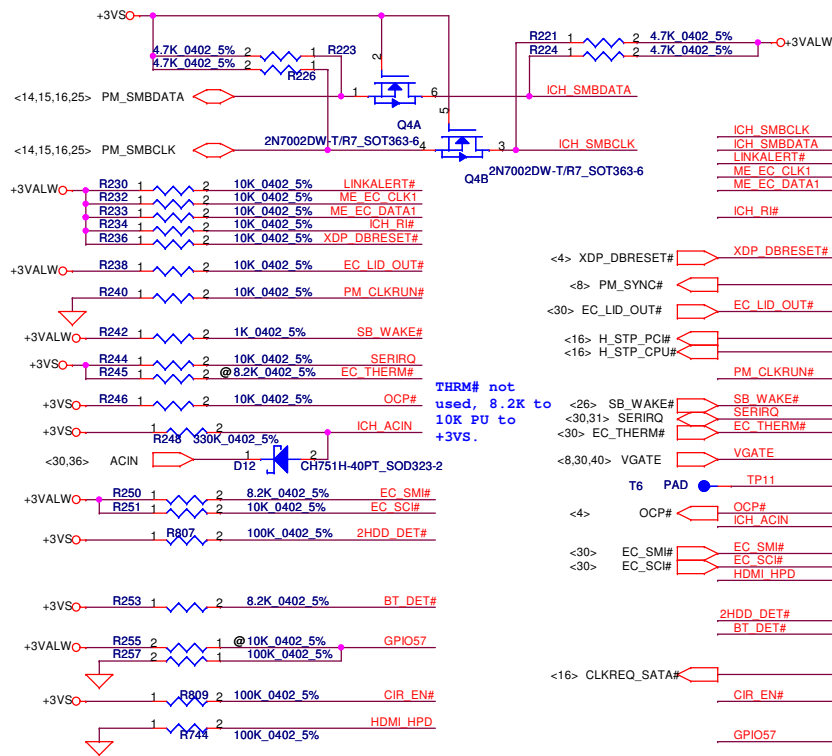
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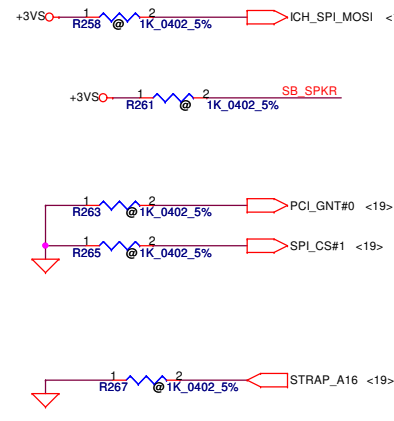
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ITPM Physical Presence	
CLGPIO5	Assert = iTPM Physical Presence Enable
Mobile Platform	De-assert = iTPM disable
GPIO57	**Only used in iAMT w/ME Firmware
GPIO57	Desktop Platform used only

## ICH9M Strap Pin

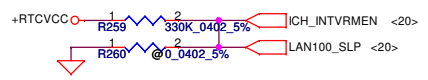


Internal TPM Strap (Internal pull-down)	
SPI_MOSI	Low= Disable High= iTPM enable by MCH strap*

No Reboot Strap (Internal pull-up)	
SB_SPKR	Low= "Default" High= "No Reboot"

Boot BIOS Strap (Internal pull-up)		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default* (Internal pull-up)



Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

XOR Chain Entrance Strap		
ICH_TP3 (Internal pull-up)	HDA_SDOUT (Internal pull-down)	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

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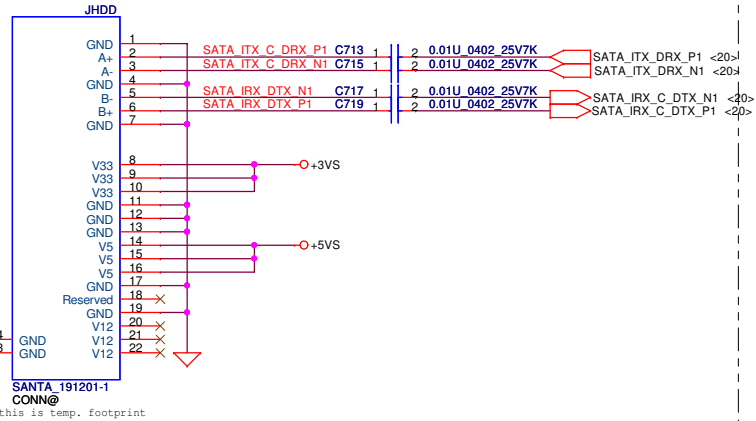
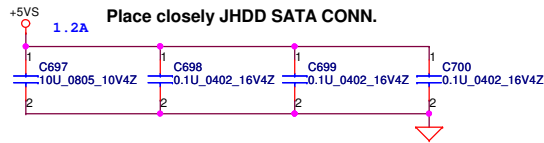






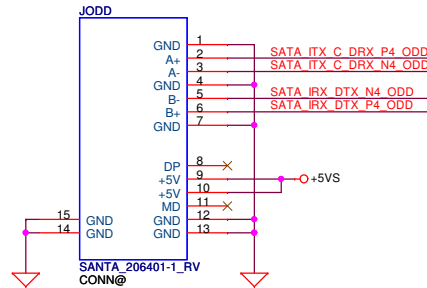
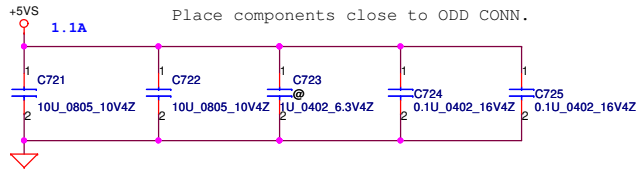
## SATA HDD Conn.

Place closely JHDD SATA CONN.

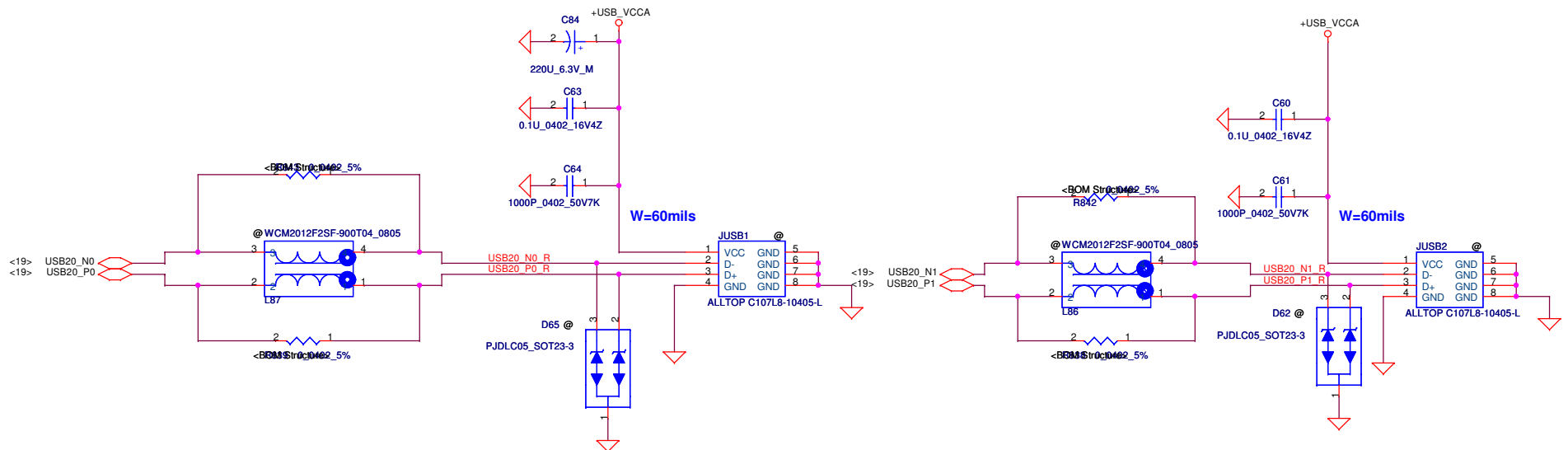


## SATA ODD Conn

Place components close to ODD CONN.



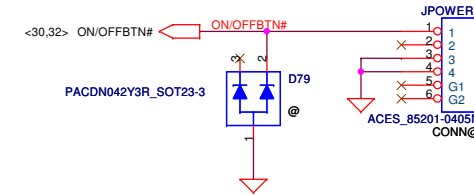
## USB Conn



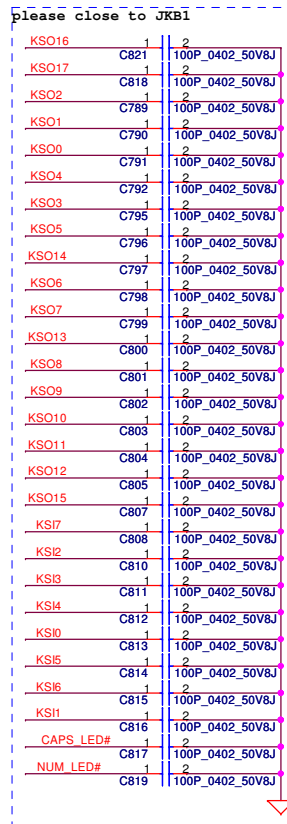
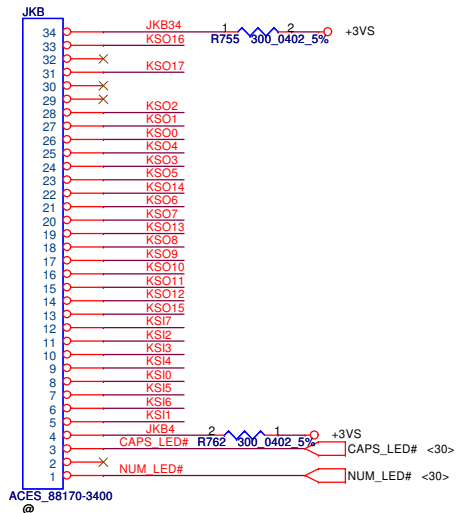
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## POWER/B Connector Check footprint and pin define

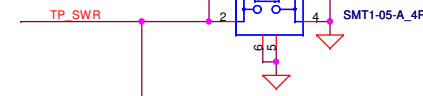


## KEYBOARD CONN

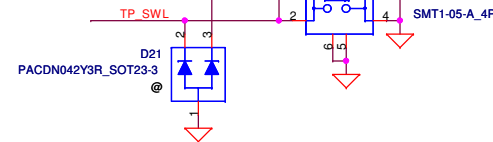


## Touch/B Connector

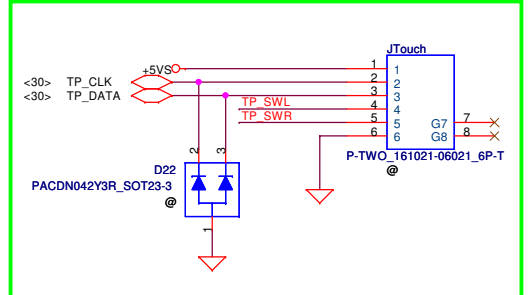
### Right Switch



### Left Switch



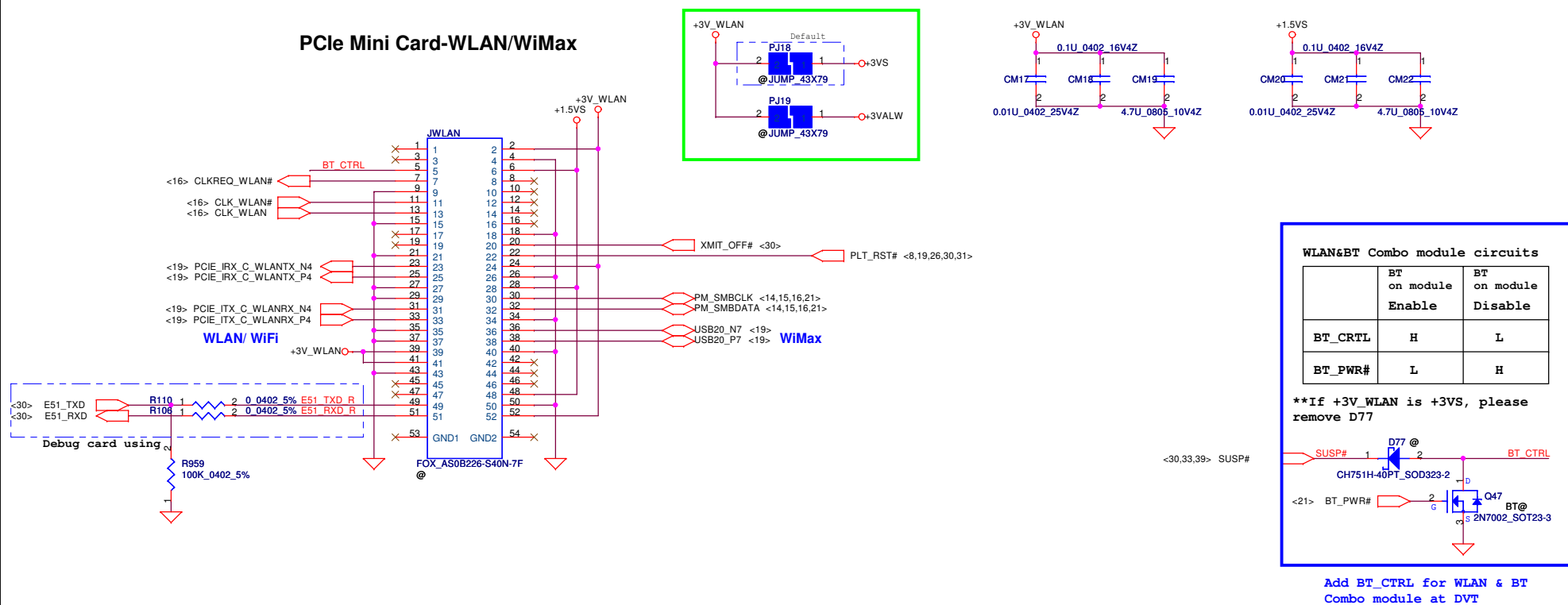
### Check signal to TP module through FFC



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# PCle Mini Card-WLAN/WiMax



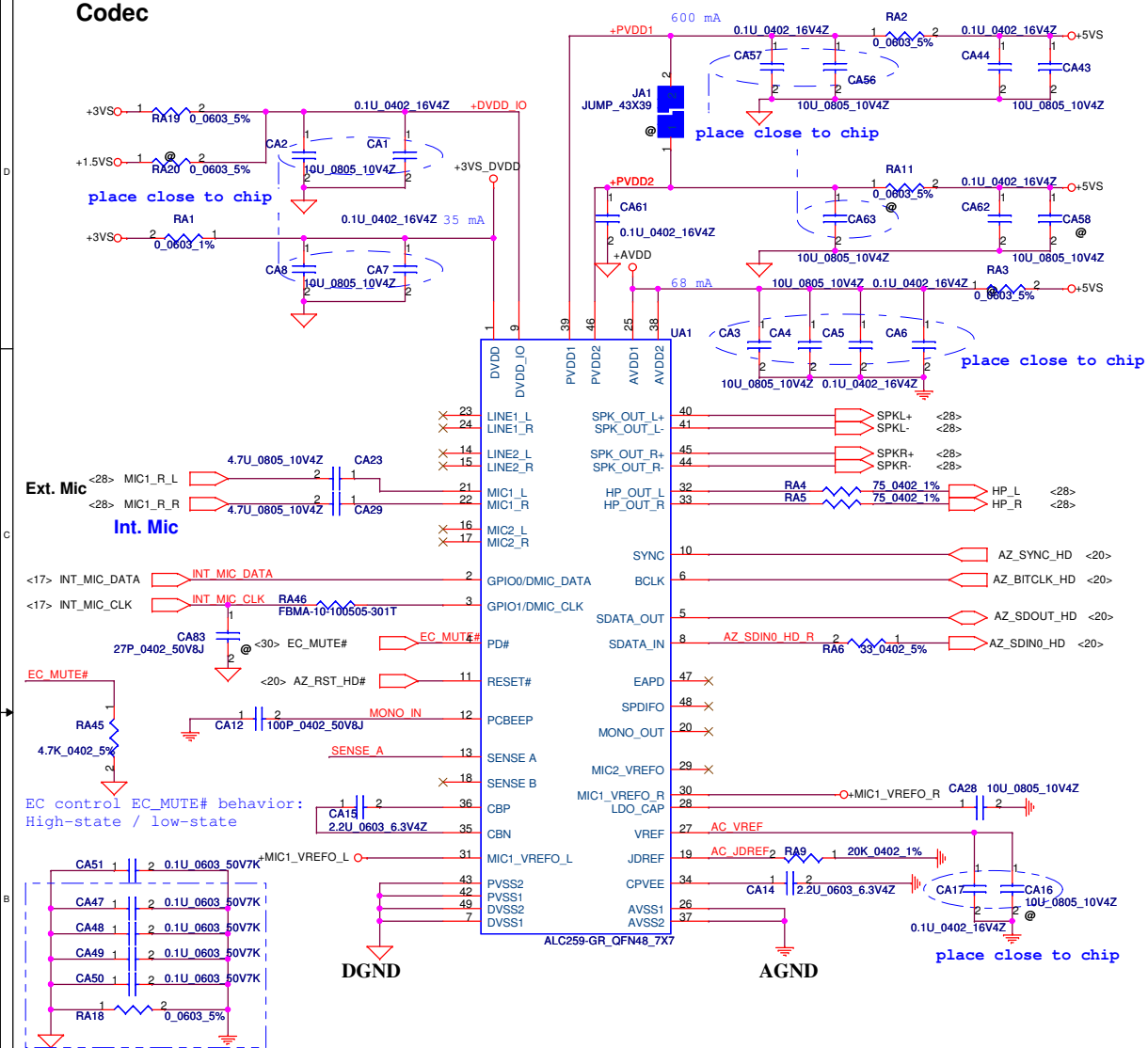
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Size		Document Number		Rev
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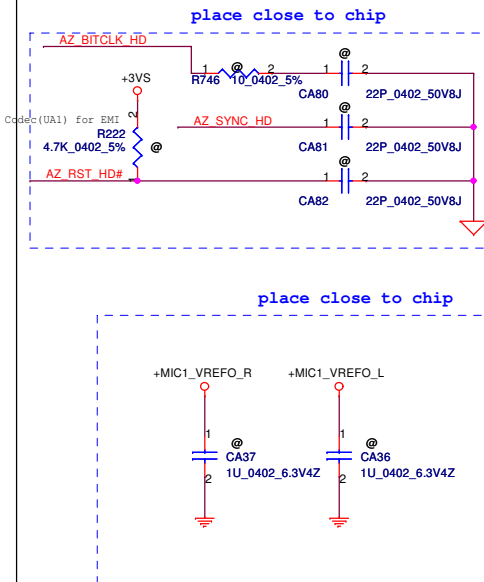
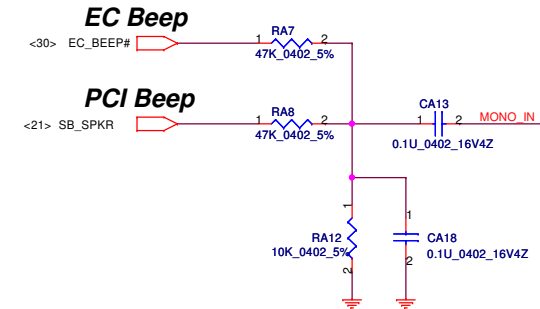




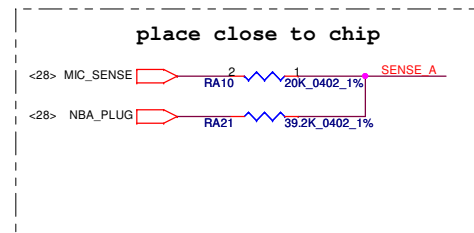
## Codec



### Beep sound



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 20)	



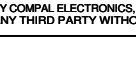
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title HD CODEC ALC272		
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					PWWAA LA6841P M/B	0.1
				Date:	Monday, August 16, 2010	[Sheet 27 of 44]



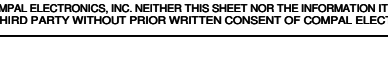
**WWW.AliSaler.Com**



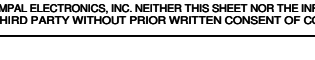
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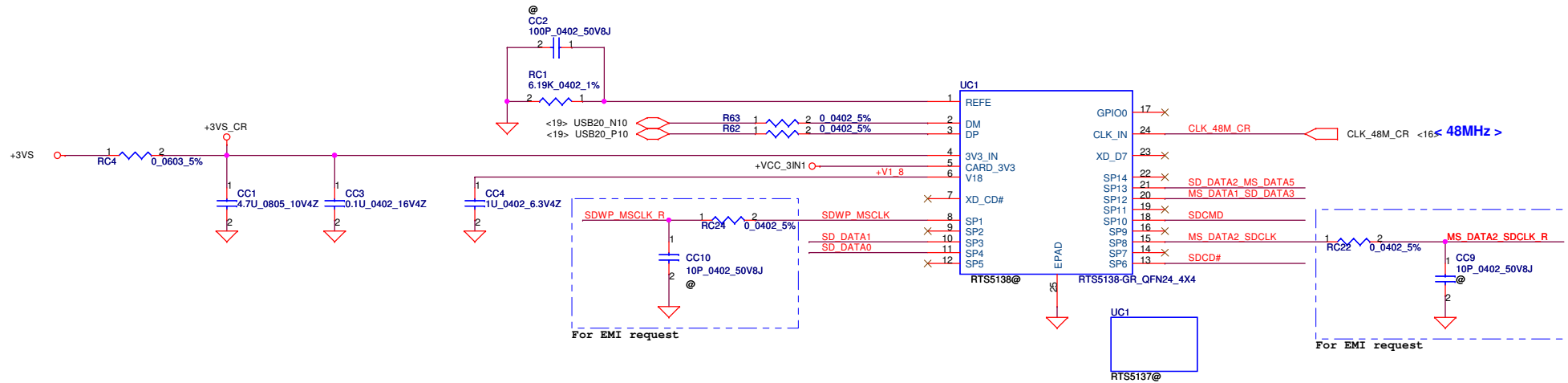


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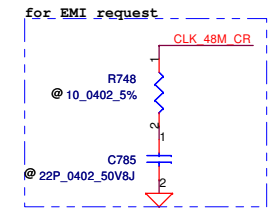
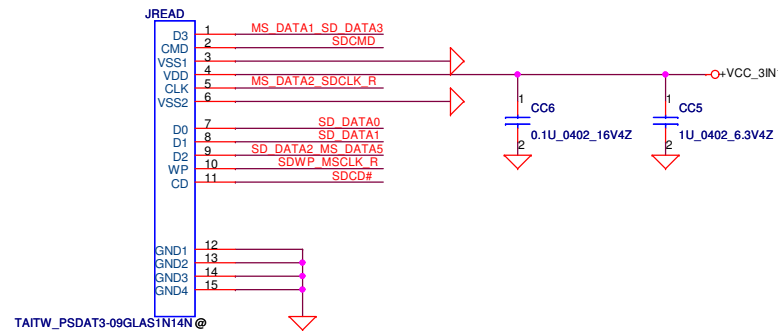


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Date: <b>Monday, August 16, 2010</b>				Sheet	28	of 44





< 2 in 1 Card Reader >



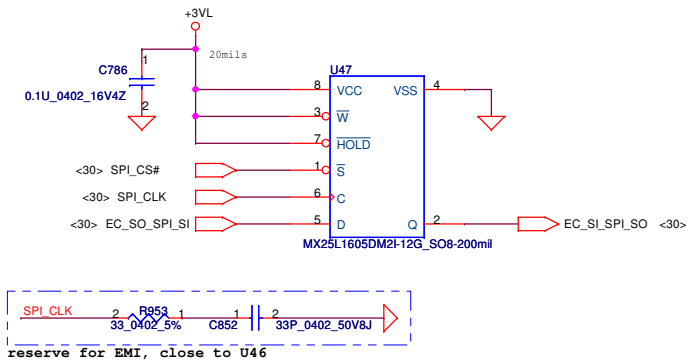
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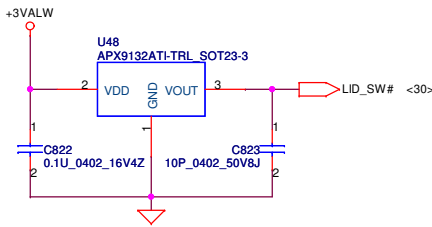




SPI Flash (16Mb\*1)

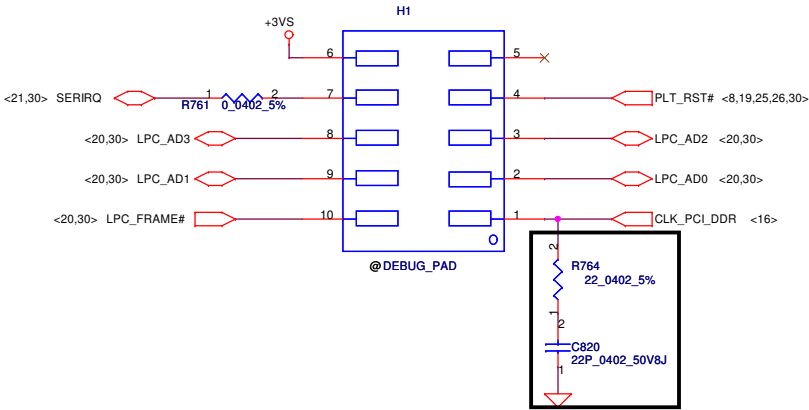


Lid SW

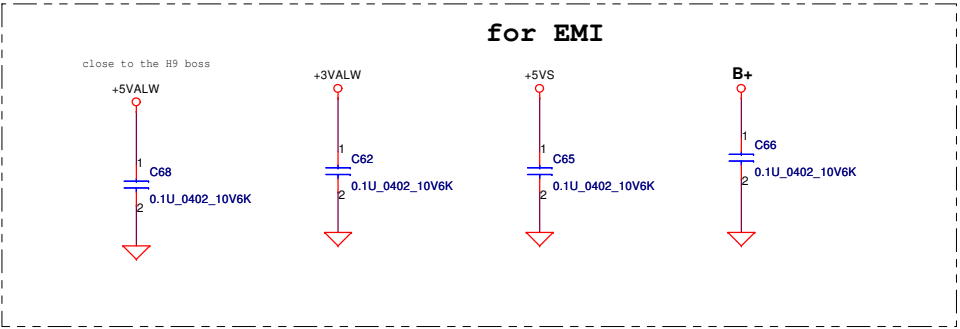


LPC Debug Port

Please place the PAD under DDR DIMM.



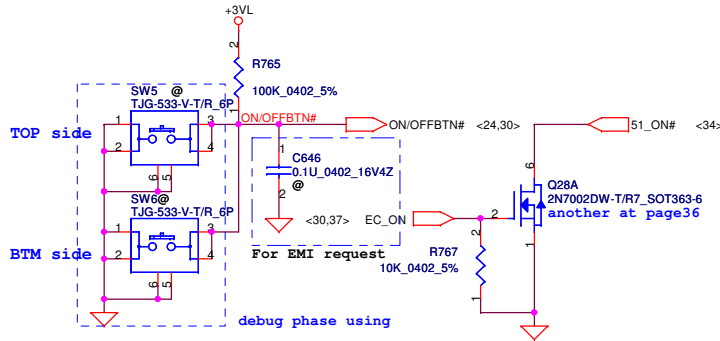
for EMI



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2009/06/12		2010/06/12		SPI ROM/TP/KB/Debug	
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Power Button

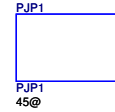


ISPD

PCB



DC-IN



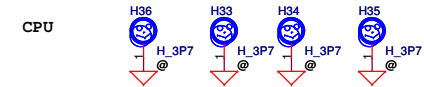
NB\_GL40\_R3

NB\_GL40\_R1

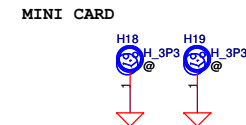
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SB\_R1

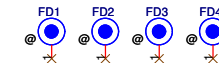
Screw Hole



SB



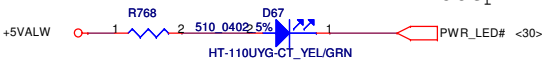
PCB Fedcal Mark PAD



DC-IN LED

Vf=2.0V (typ), 2.4V (max)  
If=30mA (max)

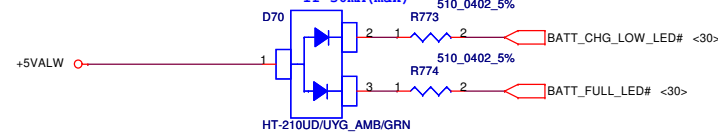
footprint is SC510UYG000



BATT CHARGE/FULL LED

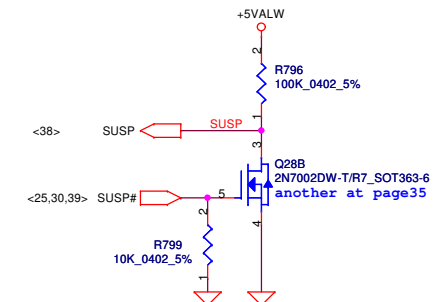
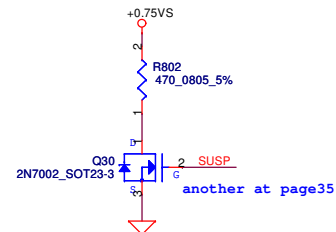
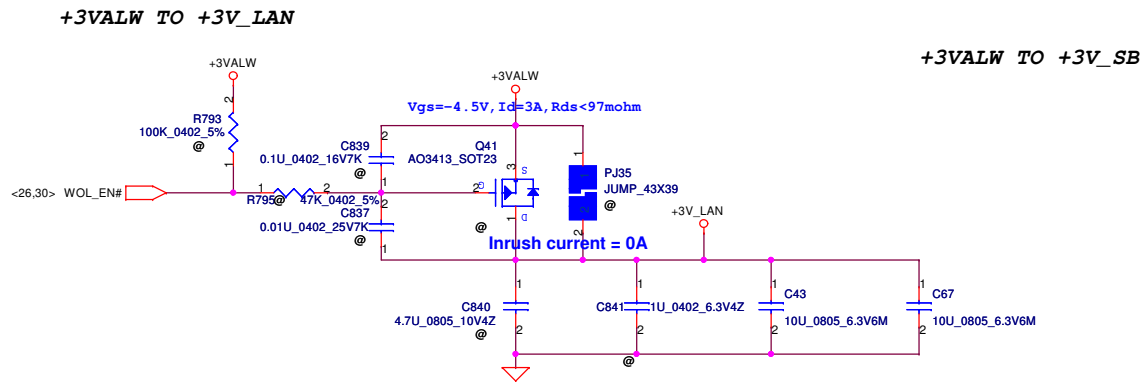
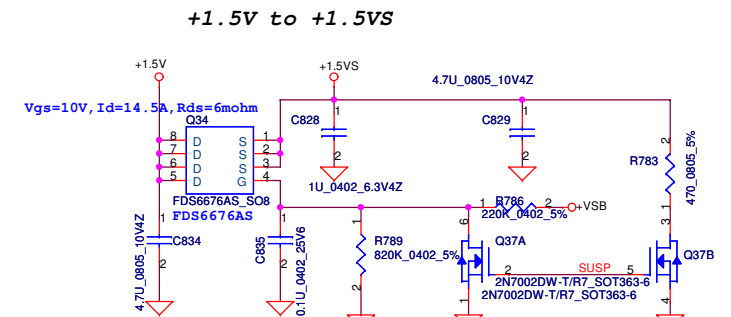
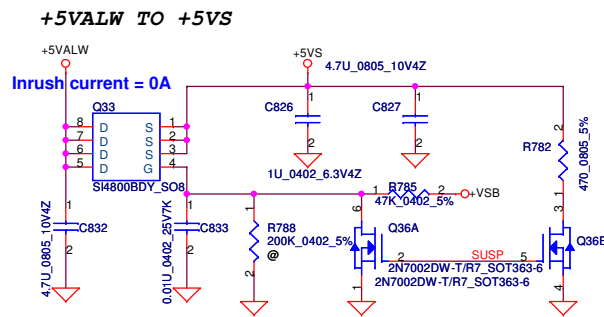
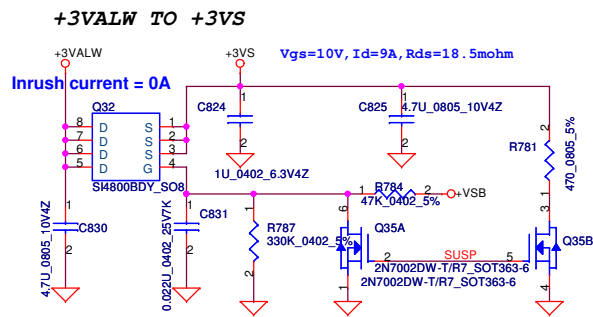
Vf=1.9V (typ), 2.4V (max) for amber  
Vf=2.0V (typ), 2.4V (max) for green  
If=30mA (max)

footprint is SC510UDG000



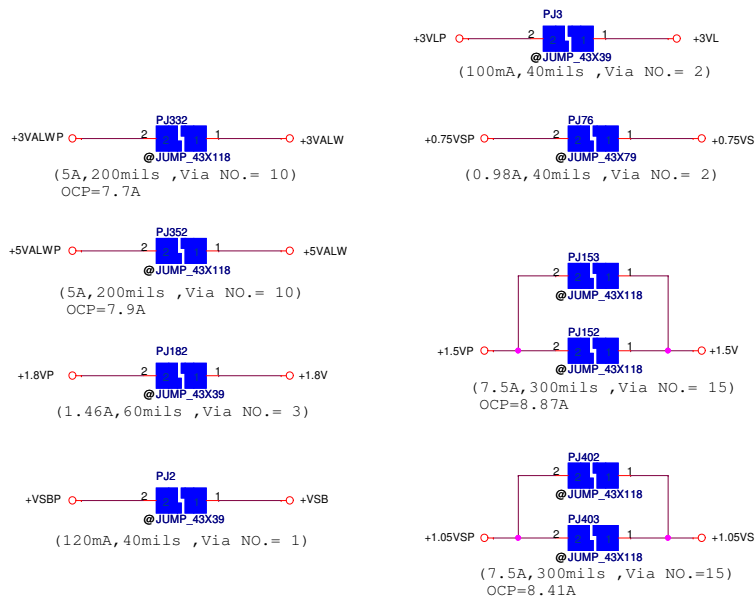
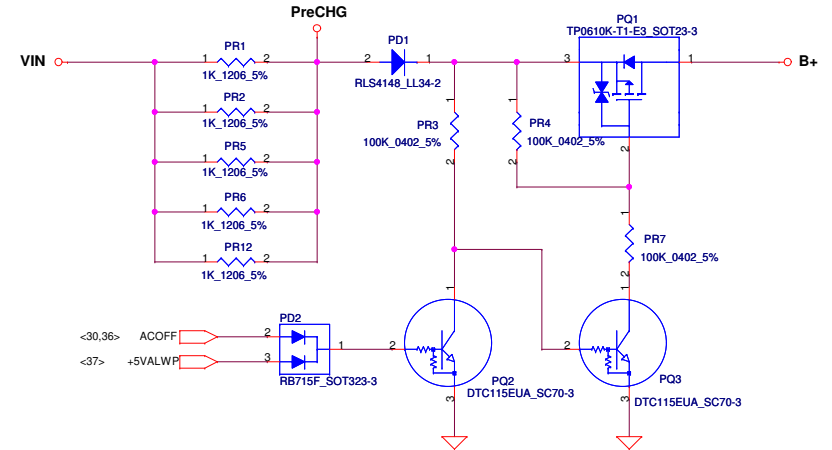
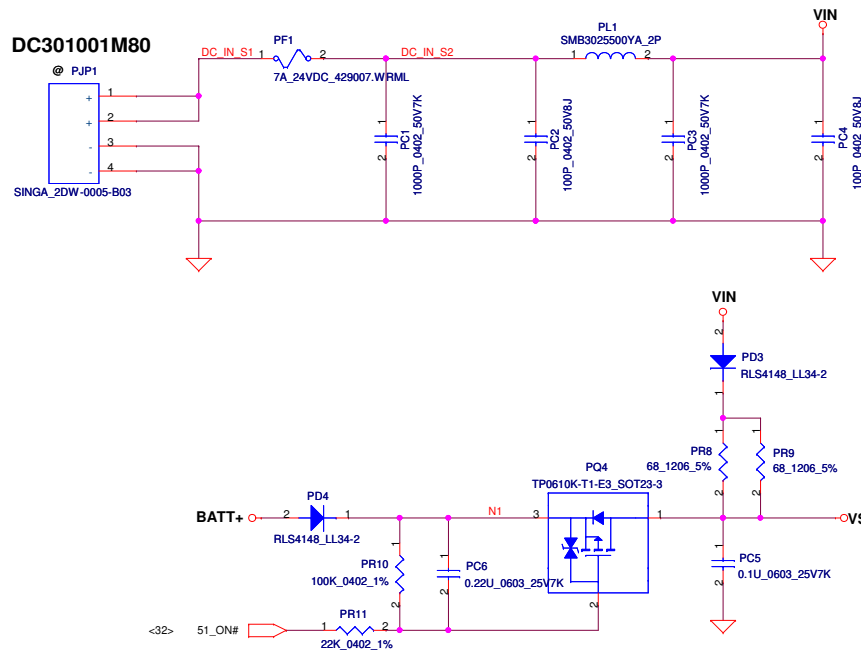
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#### ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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		Deciphered Date		DCIN & DETECTOR	
		2010/06/12		Size	
				Document Number	
				KSWAA	
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				Date: Monday, August 16, 2010	
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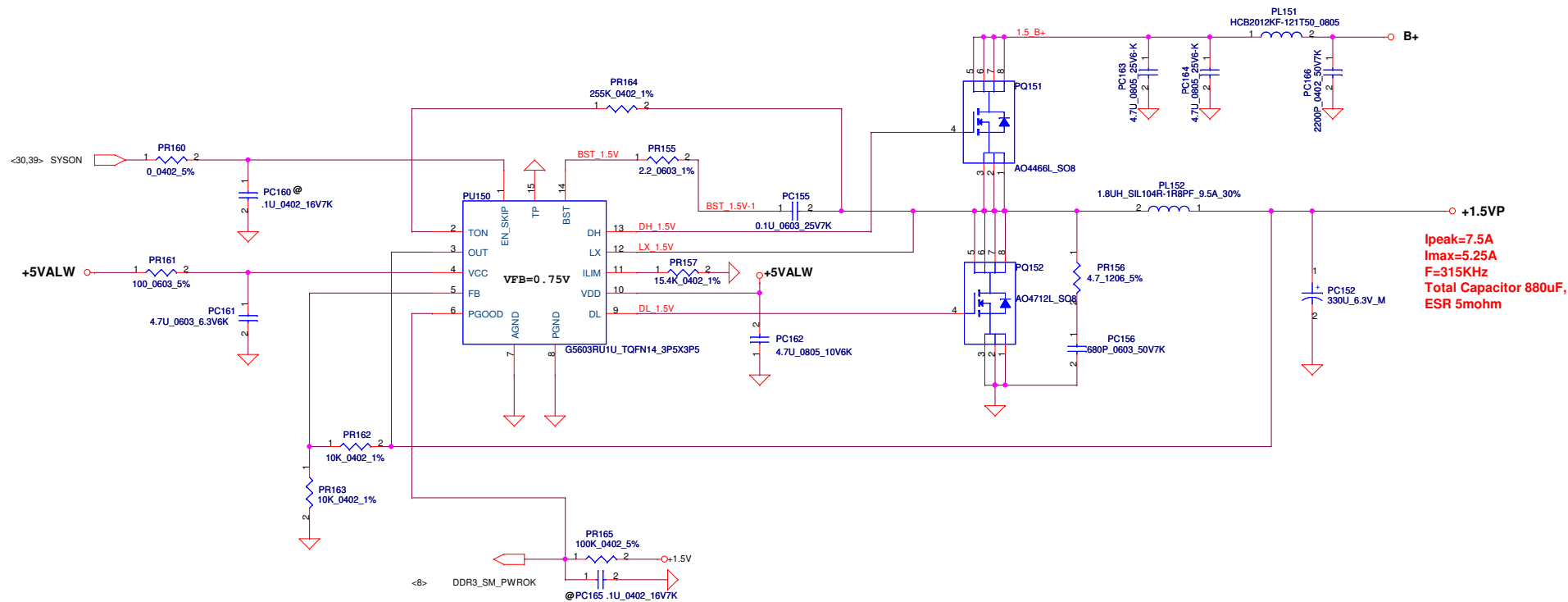






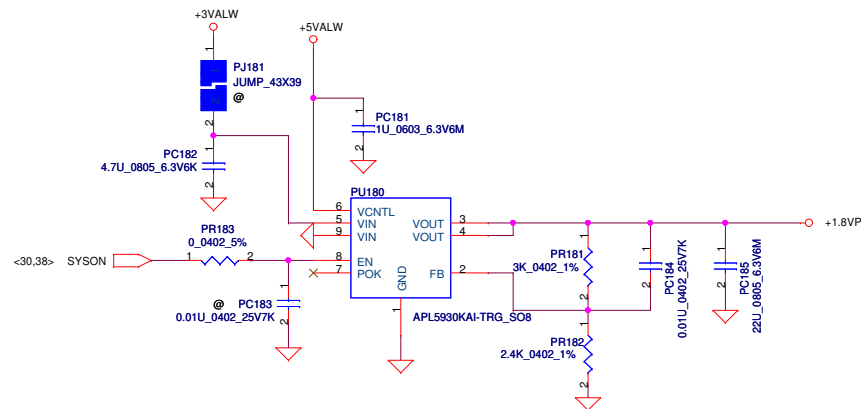
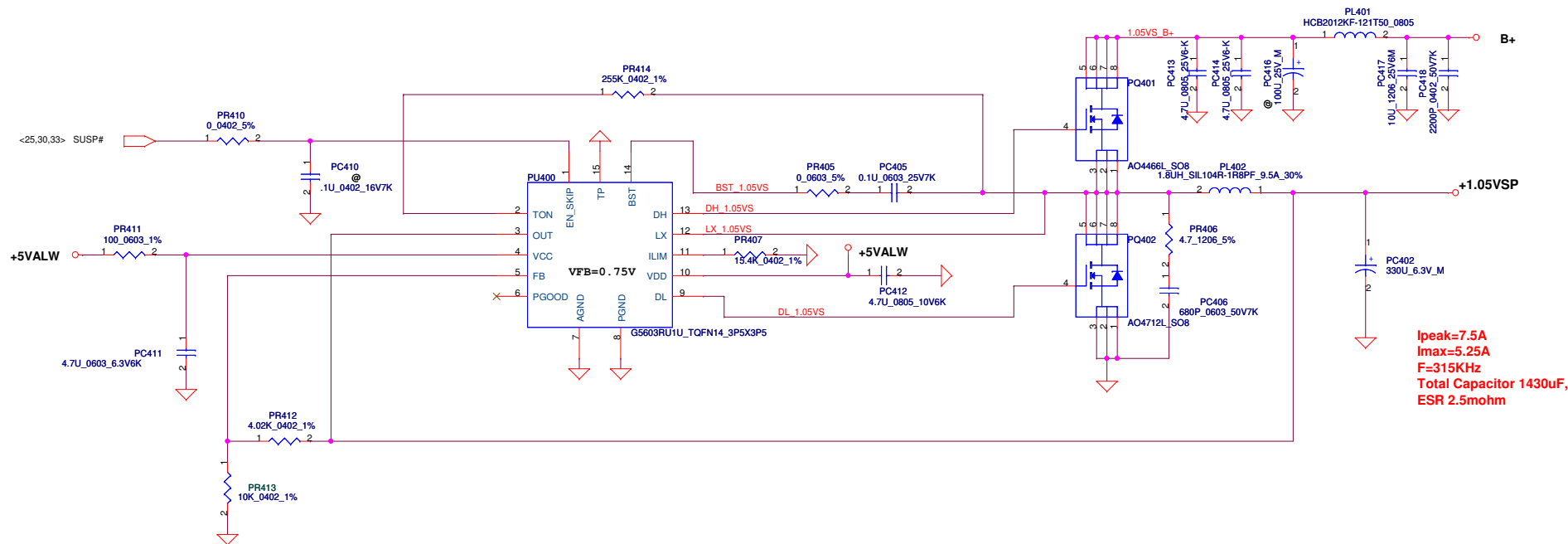






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				0.1	







PIR (Product Improve Record)

REVISION CHANGE: 0.1 TO 0.2 PVT

NO DATE PAGE MODIFICATION LIST				PURPOSE
1.	07/23	32	Change R768,R773 from 120 ohm to 510 ohm	for changed 5mA LED
2.	07/23	32	Chage LED power rail from +3valw to +5valw	for changed 5mA LED
3.	07/23	23	del. L86,L87 EMI component	for EMI request
4.	07/23	31	Add 1PCS(C62) 0.1uF_0402 on +3Valw-->GND	for EMI request
5.	07/23	31	Add 1PCS(C65) 0.1uF_0402 on +5Vs-->GND	for EMI request
6.	07/23	31	Add 0.1uF_0402(C66) on B+-->GND close to H8	for EMI request
7.	07/23	28	JLINE and JEXMIC change from DC2300006300 to DC230004L00	for SMT DFx request
8.	07/27	30	change R742 from +3VALW to +3VL	for LED no function issue
9.	07/27	8	add test pad ON U3.E36,U3.AK34	for ATE request
10.	07/27	33	change part number of Q30 (SB770020010)	for Reduce BOM part type
11.	07/27	32	Change D67(power on LED) from SC510UYG000 to SC500009D00	for changed 5mA LED
12.	07/27	32	Change D70(DC in LED) from SC510UDG000 to SC500009800	for changed 5mA LED
13.	07/29	14	un-mount CD7,CD8,CD9,CD10,CD11,CD12,CD30,CD31,CD32,CD34,and mount (22uF) CD29,CD33	for design change
14.	07/29	11	For +1.5V ,C78 from 330uF to 390u (SF000002000)	for design change
15.	07/29	12	Change R82 and R81 from inductor to Bead	for design change
16.	07/29	15	+0.75VS filter un-mount CD22 and CD44	for design change
17.	08/03	25	un-mount D77	for If +3V_WLAN is +3VS, please un-mount D77



PIR (Product Improve Record)

REVISION CHANGE: 0.2 TO 0.3 Pre-MP

NO	DATE	PAGE	MODIFICATION LIST
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PURPOSE

1.	08/09	29	Change net V1_8 to +v1_8	for power trace
2.	08/09	32	add R774	for LED control
3.	08/12	32	un-mount SW5 and SW6	for Pre-MP do need power SW
4.	08/12	20	add R16 (for RTC battery)	for design change
5.	08/13	26	add D69 and un-mount CL38	for EMI request
6.	08/13	26	CL37 from 0.1uF to 120pF	for EMI request
7.	08/13	26	add CL35	for EMI request
8.	08/13	27	add CA51	for EMI request
9.	08/13	33	add C67 and C43	for EMI request



PIR (Product Improve Record)

REVISION CHANGE: 0.1 TO 1.0

NO DATE PAGE MODIFICATION LIST

PURPOSE

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Version Change List ( P. I. R. List )for Power Circuit

Page#Item TitleSolution Description

PVT : modification from EVT		
P35	mount ESD diode	mount PD5, PD6
P36	EMI request	add PC236 10uF
P37	EMI request	add PC367 10uF, PC368 2200pF
P37	change 3/5V IC main source	change PU330 to UP6182
P38	EMI request	add PC166 2200pF
P39	EMI request	add PC417 10uF, PC418 2200pF
P40	adjust loadline	change PR535 to 3.09K
P34	unify source	change PD1 to SC11N414880
P36	unify source	change PQ216 to SB000009610
P37	unify source	change PQ362 to SB000009610
P40	unify source	change PL502 to SM010020720
P40	turn on speed too quick	change PQ502, PQ504 to MDU2653RH
P37	change cap to 330uF with same price	change PC332, PC352 to SF000002000
P38	change cap to 330uF with same price	change PC152 to SF000002000
P39	change cap to 330uF with same price	change PC402 to SF000002000
P36	EMI request to mount snubber circuit, ISN caps	add PR206, PC206; PC234, PC235
P37	EMI request to mount snubber circuit	add PR336, PC336; PR356, PC356
P38	EMI request to mount snubber circuit & boost resistor	add PR156, PC156; change PR155 to 2.2ohm
P39	EMI request to mount snubber circuit	add PR406, PC406
P40	EMI request to mount snubber circuit	add PR506, PC506; PR516, PC516
PreMP : modification from PVT		
P34	increase precharge design margin	add PR12 1K
P35	change OTP setting	change PR15 to 23.2K, PR18 to 10.7K
P35	change source	chagne PC9 to SE070104280
P37	change 3/5V IC main source	change PU330 to TP851125A
P38	change 0.75V IC main source	change PU75 to G2992
P40	adjust loadline	change PR535 to 4.53K
P40	adjust transient stability	change PR527 to 220pF

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